



FIG. 1

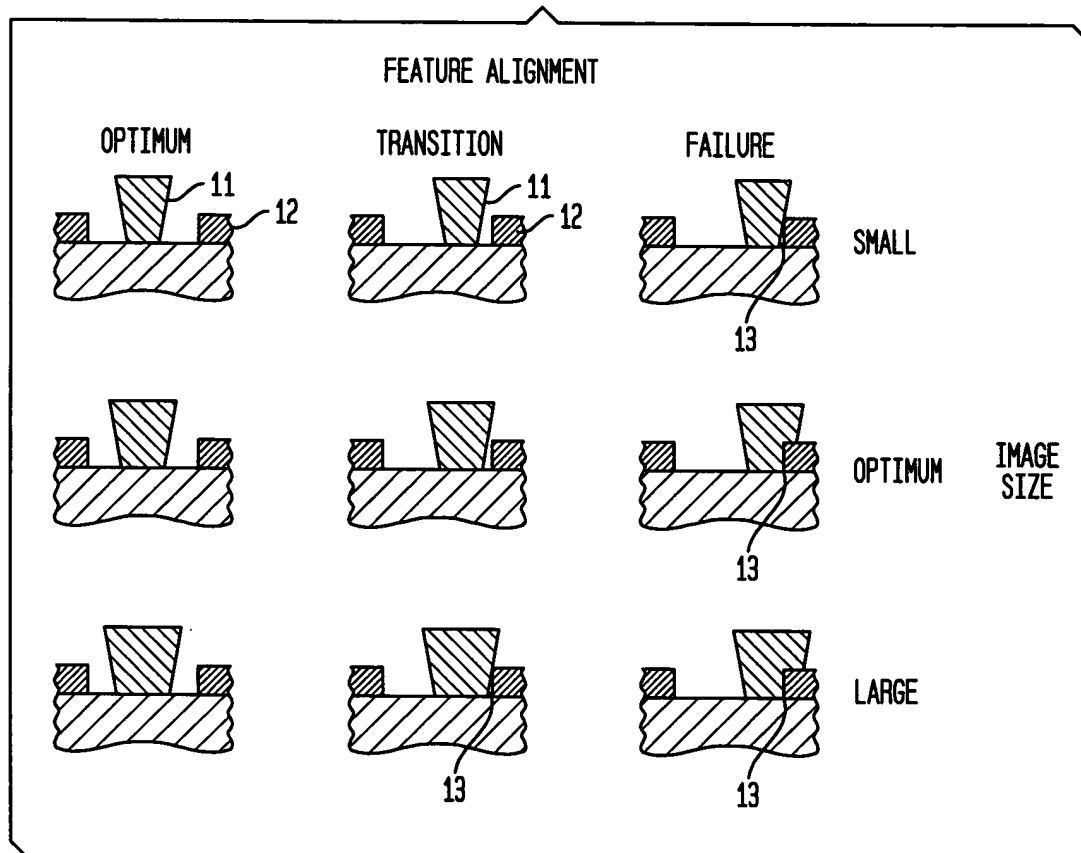


← INCREASING OVERLAY DECREASING →

|  |                    |                    |                    |                |                    |                    |                    |
|--|--------------------|--------------------|--------------------|----------------|--------------------|--------------------|--------------------|
|  | $X + 3$<br>$Y + 3$ | $X + 2$<br>$Y + 3$ | $X + 1$<br>$Y + 3$ | $X$<br>$Y + 3$ | $X - 1$<br>$Y + 3$ | $X - 2$<br>$Y + 3$ | $X - 3$<br>$Y + 3$ |
|  | $X + 3$<br>$Y + 2$ | $X + 2$<br>$Y + 2$ | $X + 1$<br>$Y + 2$ | $X$<br>$Y + 2$ | $X - 1$<br>$Y + 2$ | $X - 2$<br>$Y + 2$ | $X - 3$<br>$Y + 2$ |
|  | $X + 3$<br>$Y + 1$ | $X + 2$<br>$Y + 1$ | $X + 1$<br>$Y + 1$ | $X$<br>$Y + 1$ | $X - 1$<br>$Y + 1$ | $X - 2$<br>$Y + 1$ | $X - 3$<br>$Y + 1$ |
|  | $X + 3$<br>$Y$     | $X + 2$<br>$Y$     | $X + 1$<br>$Y$     | $X$<br>$Y$     | $X - 1$<br>$Y$     | $X - 2$<br>$Y$     | $X - 3$<br>$Y$     |
|  | $X + 3$<br>$Y - 1$ | $X + 2$<br>$Y - 1$ | $X + 1$<br>$Y - 1$ | $X$<br>$Y - 1$ | $X - 1$<br>$Y - 1$ | $X - 2$<br>$Y - 1$ | $X - 3$<br>$Y - 1$ |
|  | $X + 3$<br>$Y - 2$ | $X + 2$<br>$Y - 2$ | $X + 1$<br>$Y - 2$ | $X$<br>$Y - 2$ | $X - 1$<br>$Y - 2$ | $X - 2$<br>$Y - 2$ | $X - 3$<br>$Y - 2$ |

↑ INCREASING CD

FIG. 2



The diagram shows a cross-section of a semiconductor device. At the bottom is a thick layer labeled "WAFER". Above the wafer is a layer of "OXIDE". Within this oxide layer, there is a central rectangular region labeled "LEVEL 1" and "16". Above this central region is another layer of "OXIDE". Within this upper oxide layer, there is a central rectangular region labeled "LEVEL 2" and "17". The regions are separated by thin lines, and the entire structure is bounded by a top and bottom layer of "OXIDE".

**FIG. 5**

